RK

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte STEFAN PFAB

Appeal No. 2004-1020
Application No. 09/486,908

ON BRIEF

Before KRASS, DIXON and SAADAT, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-7 and 9-14. Claims 8 and 15 have been indicated by the examiner as being directed to allowable subject matter and are not before us on appeal.

The invention is directed to a data storage device. In particular, the invention seeks to speed up the offering of data that represent successor commands after branches in a computer

program. This increase in speed is made possible by an overlapped buffering scheme.

Representative independent claim 1 is reproduced as follows:

1. A data storage device, comprising:

memory cells having stored data with selectable output addresses;

wherein said storage device responds to a data output request by outputting said stored data beginning with a selected output start address;

wherein selectable output start addresses are spaced from one another such that an amount of data that can be stored between neighboring output start addresses is smaller than an amount of data output in response to said data output request.

The examiner relies on the following reference:

Pawlowski	5,787,475	Jul. 28, 1998

Claims 1-7 and 9-14 stand rejected under 35 U.S.C. § 102(e) as anticipated by Pawlowski.

Reference is made to the briefs and answer for the respective positions of appellant and the examiner.

OPINION

A claim is anticipated only when a single prior art reference expressly or inherently discloses each and every

element or step thereof. Constant v. Advanced Micro-Devices Inc., 848 F.2d 1560, 7 USPQ2d 1057 (Fed. Cir. 1988); RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 221 USPQ 385 (Fed. Cir. 1984).

It is the examiner's position, with respect to the independent claims 1 and 9, that Pawlowski discloses a data storage device in a main memory and I/O module, referring to column 4, lines 5-15. Referring to lines 34-45 and 54-60, of that column, as well as Figure 1, item 14, the examiner cites memory cells having stored data with selectable output addresses, "wherein the specific starting address provided by the request of data is used to determine which cache line or consecutive cache lines in memory contain a beginning portion of the requested data, and outputting the requested data with cache lines or consecutive cache lines, which are considered to be the selected output start address" (answer-page 3).

Citing column 4, lines 34-45, column 5, line 66 to column 6, line 10, and column 6, lines 19-35 and 50-59, of Pawlowski, the examiner urges that the storage device responds to a data output request by outputting the stored data beginning with a selected output start address, "wherein the specific starting address provided by the request of data is used to determine which cache

line or consecutive cache lines in memory contain a beginning portion of the request data, and outputting the requested data with cache lines or consecutive cache lines, which are considered to be the selected output start address" (answer-page 3).

For the claim limitation of "wherein selectable output start addresses are spaced from one another such that an amount of data that can be stored between neighboring output start addresses is smaller than an amount of data output in response to said data output request," the examiner points to column 6, lines 30-35, column 7, lines 15-25, column 9, line 56 to column 10, line 15, column 11, lines 45-58, and column 11, line 64 to column 12, line 8, of Pawlowski.

The examiner explains, at page 4 of the answer:

> Data retrieved by the I/O controller to determine which cache line of data contains the beginning portion of address requested by the peripheral from the memory. If this beginning portion of the address is in the first cache line, then the data output to requested data by the first cache line. However, if the retriever determines that a next consecutive cache line contains the beginning portion of the requested data, the retriever increments the starting address and uses the incremented starting address to request the consecutive cache lines of data from memory. In all situations, a first cache line of consecutive cache lines, the data stored in the neighboring starting address is less than the output address since if the portion of the starting address provided by the requested data is in the first cache line, the output transfers to requested data by first cache line; and if

> it is greater than the first cache line, the output transfers by two consecutive cache lines (sic).

Appellant contends that Pawlowski discloses a device which, in response to a data output request, outputs an amount of data that *corresponds* to the amount of data that can be stored between neighboring output start addresses, and does not output an amount of data *greater than* the amount of data that can be stored between neighboring output start addresses. Appellant maintains that Pawlowski "does not permit the access of the data storage device in amounts other than entire cache lines" (principal brief-page 7), whereas the instant invention permits an overlap of the memory regions that can be retrieved based on the output start addresses of the memory device so that multiple requests of the device may not be required when accessing an amount of memory larger than the spacing of the possible output start addresses, providing an advantage of speed.

The conflict between the positions of the examiner and appellant appears to stem from the examiner's consideration of Pawlowski's I/O module, together with the main memory, as constituting the claimed "data storage device," whereas appellant views only Pawlowski's main memory as constituting the "data storage device" of Pawlowski.

If appellant is correct, then Pawlowski does not anticipate the instant claimed invention because while the combination of the main memory and the I/O module can provide an arbitrary amount of data greater than one addressable cache line (admitted by appellant at page 8 of the principal brief), this would still require two accesses to the main memory. If the examiner is correct, the rejection will be sustained because appellant argues no other claim limitation.

We have reviewed the evidence of record and find ourselves in agreement with the examiner.

There is nothing apparent in the instant claims which would preclude the combination of Pawlowski's main memory 14 and I/O module as forming the claimed "data storage device."

As further explained by the examiner, at page 7 of the answer, Pawlowski's peripheral 28 issues a data request to the main memory/I/O Module combination. See column 2, lines 30-35, of Pawlowski, where it states that the peripheral may request less than a cache line of data in one transaction or it may request greater than a multiple number of cache lines of data in a transaction. Accordingly, appellant's contention that Pawlowski does not permit the access of the data storage device in amounts other than the entire cache line would appear to be

inaccurate, as the background section of the reference clearly indicates otherwise.

As explained in column 7, lines 15-30, of Pawlowski, while the first cache line of data is being retrieved, the I/O controller may cause the prefetch of consecutive cache lines of data. Thus, while the main memory is retrieving the first cache line of data, the combination of the main memory and the I/O module results in the access of a "data storage device" in amounts other than the entire cache line.

Moreover, we agree with the examiner's reasoned analysis, at pages 7-8 of the answer, wherein the examiner explained that the amount of data that can be stored between two neighboring starting addresses, e.g., starting addresses A & B, would be a single cache line. A request resulting in the output of both the initial cache line (cache line 1) and a prefetch line (cache line 2) would therefore output two cache lines. Thus, the amount of data that can be stored between two neighboring start addresses, viz., one cache line, would be smaller than the amount of data output in response to the request, viz., two cache lines.

Appellant's response is merely to argue that the examiner's interpretation of the combination of the I/O module and the main memory comprising a "data storage device" is "inconsistent with

how one of ordinary skill in the art would interpret a 'data storage device'" (reply brief-page 2). Yet, appellant never explains *why* the skilled artisan would not consider a plurality of combined elements a "device" or why a data storage device cannot include a main memory module, an I/O module separate therefrom, and a bus therebetween to permit communication between these two entities. After all, many "devices" are made up of a composite of individual elements. Therefore, we find it quite reasonable that a "data storage device" may comprise other elements, such as a main memory, an I/O module, and a bus therebetween, especially where the instant claims do not preclude the device from comprising these elements.

Appellant contends, at page 4 of the reply brief, that the term, "data storage device" is defined in the specification as being a "program memory", and not some aggregation of computer component devices.

First, we note that appellant has not indicated exactly where, in the specification, such a definition can be found. But, even so, where, as here, the claimed term is clear, it is given its plain and ordinary meaning. It is not apparent that a separate meaning is intended, and it is not necessary to refer to the specification for a meaning other than the plain and ordinary

meaning of a "device." Moreover, assuming, arguendo, we are to give the claimed "device" the meaning of a "program memory," as urged by appellant, there is no reason why a program memory cannot comprise more than a single element.

Further, even appellant admits that page 3, lines 14-15, of the instant specification indicates that "the data storage device can also fundamentally be a matter of other, arbitrary data storage devices." We do not agree with appellant that this language would be understood by the artisan as "still requiring some form of an integrated device." Integration has never been indicated as being a criterion of the claimed storage device.

Since appellant has not convinced us of any error in the examiner's position, we will sustain the rejection of claims 1-7 and 9-14 under 35 U.S.C. § 102(e).

The examiner's decision is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

ERROL A. KRASS)
Administrative Patent Judge)
)
)
)
JOSEPH L. DIXON) BOARD OF PATENT
Administrative Patent Judge) APPEALS AND
) INTERFERENCES
)
)
MAHSHID D. SAADAT)
Administrative Patent Judge)

EK/RWK

Appeal No. 2004-1020
Application No. 09/486,908

SCHIFF HARDIN & WHITE
PATENT DEPARTMENT
7100 SEARS TOWER
CHICAGO, IL 60606-6473